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Claims

[c1] A method of forming an array of DRAM cells comprising the steps of:
forming trench capacitors in a first set of trenches in a semiconductor substrate;
forming vertical transistors above said trench capacitors in said first set of trenches, said capacitors and vertical transistors being connected by a set of buried straps formed at a strap depth in a layer of said semiconductor substrate;
forming a second set of trenches in said semiconductor substrate, said second set of trenches being disposed between members of said first set of trenches, said second set of trenches having an insulating liner at said strap depth, whereby potential paths between adjacent buried straps in said first set of trenches are blocked from forming; and
said second set of trenches contain a vertical conductive path connecting body regions in said semiconductor substrate at a level above said strap depth and bias regions in said semiconductor substrate at a level below said strap depth.

[c2] A method according to claim 1, further comprising the steps of:
etching said trenches within upper and lower regions of a well, such that said upper and lower regions of said well are connected by a conductive path.

[c3] A method according to claim 1, further comprising the steps of:
forming a liner on the interior surfaces of said second set of trenches; and
etching said liner on the bottom surface of said second set of trenches, so that said conductive path extends to said substrate through said bottom surface.

[c4] A method according to claim 2, further comprising the steps of:
forming a liner on the interior surfaces of said second set of trenches; and
etching said liner on the bottom surface of said second set of trenches, so that said conductive path extends to said substrate through said bottom surface.

[c5] A method according to claim 1, further comprising the steps of:
filling said second set of trenches with a conductive material and diffusing said conductive material into said substrate.

[c6] A method according to claim 2, further comprising the steps of:
filling said second set of trenches with a conductive material and diffusing said conductive material into said substrate.

[c7] A method according to claim 3, further comprising the steps of:
filling said second set of trenches with a conductive material and diffusing said conductive material into said substrate.

[c8] A method according to claim 4, further comprising the steps of:
filling said second set of trenches with a conductive material and diffusing said conductive material into said substrate.

[c9] A method according to claim 1, in which said substrate is silicon and further comprising the steps of nitriding the interior surface of said second set of trenches before said step of filling said second set of trenches with a conductive material.

[c10] A method according to claim 2, in which said substrate is silicon and further comprising the steps of nitriding the interior surface of said second set of trenches before

said step of filling said second set of trenches with a conductive material.

[c11] A method according to claim 3, in which said substrate is silicon and further comprising the steps of nitriding the interior surface of said second set of trenches before said step of filling said second set of trenches with a conductive material.

[c12] A method according to claim 4, in which said substrate is silicon and further comprising the steps of nitriding the interior surface of said second set of trenches before said step of filling said second set of trenches with a conductive material.

[c13] A method according to claim 1, in which said second set of trenches are formed with a transverse dimension that is the minimum distance permitted by lithography.

[c14] An integrated circuit including an array of DRAM cells comprising:
an array of trench capacitors in a first set of trenches in a semiconductor substrate;
said array of DRAM cells further comprising vertical transistors above said trench capacitors in said first set of trenches, said capacitors and vertical transistors being connected by a set of buried straps formed at a strap

depth in a layer of said semiconductor substrate;
a second set of trenches in said semiconductor substrate, said second set of trenches being disposed between members of said first set of trenches, said second set of trenches having an insulating liner at said strap depth, whereby potential paths between adjacent buried straps in said first set of trenches are blocked from forming; and
said second set of trenches containing a vertical conductive path connecting body regions in said semiconductor substrate at a level above said strap depth and bias regions in said semiconductor substrate at a level below said strap depth.

[c15] An integrated circuit according to claim 14, in which:
said second set of trenches extend between upper and lower regions of a well and have a liner on the interior surfaces thereof, such that said upper and lower regions of said well are connected by a conductive path that is isolated from intermediate levels of said well.

[c16] An integrated circuit according to claim 14, in which said semiconductor substrate is silicon and said conductive path passes through a nitrided silicon surface above said liner.

[c17] An integrated circuit according to claim 14, in which said

semiconductor substrate is silicon and said conductive path passes through a nitrided silicon surface above said liner.